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THE MICROCOMPUTER BASED LANGUAGE LABORATORY
TEST SCORING SYSTEM DESIGN

Kuo-En Huang (黃國恩)

INTRODUCTION

Most of the ordinary language laboratory systems (or LLS) are
emphasized on developing student's hearing and speech facilities, since
both of which are essential to the mastery of any foreign languages.
However, if without some expensive test scoring machines such as mark
reader with computer and printed answer sheets get ready beforehand,
it becomes very difficult for the teacher to evaluate students on their
listening comprehension. Thus, in this article we will try to design
a test scoring system based on AIM65 microcomputer which can be attached
to any kind of LLS to perform the grading task.

In the first part of this article we will study the circuits of this
LLS and try to find some isolated lines between the master console and
the student booth for communication use. Next, we are going to design
a transmitter which will transfer the modulated digital data of student
answer to the teacher and the receiver which interfaces the microcom-
puter.

In the second part we are going to build up the system software
which includes an arithmetic unit, an interactive user interface for
setting up scoring rules, the grading and sorting subroutines and
finally the score listing program which will print out the student
marks with different format by request.
HARDWARE DESCRIPTION

I. THE AUDIO SYSTEM

The audio system under consideration is a National Audio Active Comparative Language Laboratory System which includes a Master Control Console (type WE-5100N) and 60 Student Booth Recorders and one set of stereo turntable system. The student booth recorders are 4-track,2-channel systems each equipped with a program selector offers a choice of 4 different programs, a call button to call teacher and a masking circuit to reduce the program level automatically for clear teacher/student communication without imparing the recording level. The system connection is shown in Figure 1.

![Figure 1: The audio system connection](image)

After careful examination we found that all the CALL lines are isolated from the audio signal. Thus, our efforts to design a test scoring system for this LLS will become vary simple if we use these CALL lines as the data communication bus. During the test students need only to push some buttons on the booth to tell their choice of answer. Then the message will be received by the computer through these CALL lines. Now, what rest to do is to design a circuit which will generate some sorts of coded signals to represent student's answers and the interface needed by
the computer to select student one by one. Figure 2 shows these block diagram.

Figure 2. Block diagram for system hardware

II. THE MICROCOMPUTER

The microcomputer is based on the ROCKWELL AIM65, because it is the cheapest microcomputer which can perform all the functions we want in the scoring task. (Note: without floppy disk and additional output printer, the cost is extremely low.)

The AIM65 we used in this system consists of three modules: the master module, the keyboard module and the external memory module. The master module holds a 5*7 dot matrix printer, a 20 characters display, a R6502 CPU, 20K bytes of ROM, 4K bytes of RAM and a user's R6522 VIA for I/O. The keyboard module contains a 54-key full-size keyboard with 70 functions, the external memory module contains 16K bytes of RAMs which can hold 250 problem answers for 60 students each.

The user's I/O (R6522) has two ports as shown in Figure 2. We use port A to collect student answer and port B to select student's CALL line.

III. TRANSMITTER DESIGN
1. Debouncing circuit and the keyboard encoder

We require that the keys on the student input terminal are true/false, 5 choice and C (clear). Consequently, we need at least 3 bits to tell which one of key is closed. Furthermore, since all data must be transmitted through CALL line in series, if we want to clock the status code in a cycle continually during transmission, we will need some sequence detection bits to tell the beginning of the information. This can be done by introducing "0llll" bit sequence before the encoded information bits as shown in Figure 3.

In Figure 3, the SN74148 IC is an 8 to 3 binary encoder which encodes the key status into a 3-bit binary code. The "G's" output of this IC always become "Low" whenever the key is closed. This "H" to "L" transition will trigger the next stage of 74121 IC which is a monostable multivibrator being used for keyboard debouncing ($t_w = 22\text{ms}$). The output of 74121 is connected to the next SN74123 IC. Inside 74123 there are two 74121's. The first one with $t_w = 0.72\text{ms}$ its $\overline{Q}$ signal will parallel load the status bits into 74165 shift register, while the second one generates a 3.32 sec pulse to disable 74148's input during data transmission. Note that, the parallel input pins D, E, F, G, H of 74165 are set as "01111" and the output of 74165 is fed back to its serial input terminal.

2. Pulse Width Modulation and the clock circuit.

Look at the clock circuit we construct in Figure 3. LM555 timer is operated in the astable mode to generate a sequence of unbalanced square wave with frequency calculated below:

$$f = \frac{1}{T} = \frac{1.44}{(R_a + 2R_b) \cdot C} = 1460\text{Hz}$$

$$T = 0.685\text{ ms}$$

$$t_1 = 0.693(R_a + 2R_b) = 0.42\text{ms}$$

$$t_2 = 0.693R_b \cdot C = 0.264\text{ms}$$

This clock drives the 74165 shift register to move in a cycle and also "NAND" with 74165's output $Q_h$ for modulation.

The function of 74121 as a P.W. Modulator can be explained as follows: See Figure 4, since the clock pulse is "NAND" with 74165's output $Q_h$, the clock pulse will be inverted whenever $Q_h$ is "High". Next, we use this inverted clock to trigger 74121 and output a shorter pulse $E$ ($T_w = 0.295\text{ms}$) during the clock interval. Then, if we take the same part of $E$ pulse interval away from the clock pulse, we will be able to use the rest part to represent logic "1" which is short than the clock (represent logic "0").
IV. QUESTION DETECTION CIRCUIT.

In our system we need a pulse signal to tell the computer to start scanning and collecting student's new answer at the beginning of a new question. This is done by the following circuit shown in Figure 5.
In Figure 5, the transistor $Q_1$ is turned on whenever the level detector (LM339 OP Amp) found the audio input level is higher than 0.4V. Then, $C_1$ will be grounded and this will make the second OP Amp has no output keeping the 74121 IC stand still. But if the audio signal stops, $Q_1$ will be cut off and make $C_1$ start charging through the 100K variable resistor (it takes 1 to 6 sec). Once the voltage of $C_1$ reaches 2.5V the second LM339 will turn on and triggers the 74121 to output a pulse signal to AIM65.

V. THE MULTIPLEX CIRCUIT FOR THE MICROCOMPUTER

The multiplex circuit in this system for student selection are SN74150 and 74155, see Figure 6. We use PA0 -PA3 four output lines to select one of the 16 channels in 74150 and use one of the outputs of 74155 to choose the 74150 chips. The 74155 is a 2 to 4 binary decoder which decodes PA4 and PA5 control signals. Figure 6 also shows the interface circuit used for connection of the mark reader. (MODEL EMR-A RICOH DENSHI Co. Ltd.) This mark reader will simplify the correct answer input procedure for each course.

SOFTWARE DESCRIPTION

1. SOFTWARE DEMODULATION

The modulated data of student answer are transmitted through each call line to the multiplex bus selector (see Figure 6). The selection of students is performed by port 8 of VIA6522 under the AIM65 program control. After the microcomputer completes the data collection, the demodulation technique in our system now is also done by software. First, we generate a 20 $\mu$s time base for distinguishing the signal "ON" time and "OFF" time. Next, we count the input sequence until we find the leading identification bits. Once we catch it, we will jump out of the sequence detection subroutine and put the tailing information bits into X register. If the student has not reply yet, we will put "FP" code in X register or if the student is absent we will put "FE" in it before we return from subroutine. Fig. 7 shows the flow chart of this program.

II. BASIC CONCEPTS OF THE SCORING SYSTEM

1. Interactive operation consideration

Since the audio laboratory system users are mainly English teachers, they can not operate any microcomputer which needs some complicated procedures or petty low level languages. Thus, this scoring system must be operated interactively with the teacher through some easy user
interfaces. Under this concept, we design the system software as the flow chart shown in Figure 8. In this figure, all programs will go to the next function by pressing "@" key or some special user defined keys (The AIM65 offers $F_1$, $F_2$ and $F_3$). Figure 9 is the "COURSE NAME" input subroutine. Fig. 10a is the memory map of % marks for each section in a course. Fig. 10b shows the flow chart of "% ASSIGNMENT" input program and Fig. 11 is the "LISTING" flow chart.
Figure 7. The flow chart of demodulation program
Figure 8. The flow chart of interactive operation system programs.
Figure 9. Course name input subroutine.
0244

<table>
<thead>
<tr>
<th>TN1</th>
<th>Total number of problems in this course (4 digits in decimal).</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN2</td>
<td>--- Total number of problems in this section.</td>
</tr>
<tr>
<td>PN1</td>
<td>--- &quot;1&quot; means we will deduct marks when the answer is wrong.</td>
</tr>
<tr>
<td>0/1</td>
<td>means + 25.68 when answer is right.</td>
</tr>
<tr>
<td>25</td>
<td>means - 00.75 when answer is wrong.</td>
</tr>
<tr>
<td>68</td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td></td>
</tr>
<tr>
<td>7.5</td>
<td></td>
</tr>
</tbody>
</table>

024c

| PK2 | \( PN1 + PN2 + PN3 + \ldots = TN1 \times TN2 \) |

Figure 10a. Memory map of % marks for each section in a course.

Figure 10b. The flow chart of % input subroutine.

```
Start
F2

Display: "INPUT % NOW! C = "

Wait for the course number input

=number =@?

No

Yes

Jump to start test subroutine

Store course number and calculate the corresponding % starting address.

/```

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Figure 10b. continue from the previous page.
Figure 11. The flow chart of listing subroutine.
2. The memory map

The memory map of this test scoring system is shown in Figure 12. Addresses $8000 - FFFF$ are reserved for the AIM65 system monitor. The ROM addresses $D000 - DPFF$ are allocated for our main control program of the test scoring system. Except those on-board RAM, we use off-board expansion addresses $6000 - 9FFF$ to store the student answers.

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>DAC</td>
</tr>
<tr>
<td>0001</td>
<td>decimal AC</td>
</tr>
<tr>
<td>0100</td>
<td>SP</td>
</tr>
<tr>
<td>01FF</td>
<td>Stack</td>
</tr>
<tr>
<td>0200</td>
<td>INPUT TEMP</td>
</tr>
<tr>
<td>0242</td>
<td>Input temporary storage.</td>
</tr>
<tr>
<td>0244</td>
<td>% ASSI.</td>
</tr>
<tr>
<td>0345</td>
<td>% mark assignment.</td>
</tr>
<tr>
<td>0460</td>
<td>COURSE NAME</td>
</tr>
<tr>
<td>046F</td>
<td>TEMP CORR.</td>
</tr>
<tr>
<td>0470</td>
<td>ANS. STORAGE</td>
</tr>
<tr>
<td>06AF</td>
<td>Temporally correct answer storage.</td>
</tr>
<tr>
<td>06B3</td>
<td>RECORD OF SCORE</td>
</tr>
<tr>
<td>0FFF</td>
<td>Record of student score.</td>
</tr>
<tr>
<td>6000</td>
<td>STORAGE FOR ANS.</td>
</tr>
<tr>
<td>9FFF</td>
<td>Storage for student answer.</td>
</tr>
<tr>
<td>A000</td>
<td>AIM65 I/O and RAM</td>
</tr>
<tr>
<td>AFFF</td>
<td>GRADING SYSTEM MONITOR</td>
</tr>
<tr>
<td>D000</td>
<td></td>
</tr>
<tr>
<td>DFFF</td>
<td></td>
</tr>
</tbody>
</table>

Figure 12. The memory map.

3. Arithmetic unit consideration.

Although there are many kind of IC arithmetic unit available at present time, but if we estimate the total cost by the necessary calculation we want (or the cost/performance ratio), it is not economic to use them in this system. Thus, we developed here a decimal multipression arithmetic program for the scoring use. It takes about 1.5K of memories ($D000 - D5EA$).
CONCLUSION

The test scoring system after we test it with several sample courses seems perfect in its operation. For the teacher this system provides instant feedback to pinpoint study emphasis and permit rapid student evaluation.

Although the system designed here is based on National LLS. The other LLS such as SONY, AIWA etc. can also accept it with or without isolated CALL line. Since the data transmission rate is not high, house wiring communication technique can be used for this purpose.

Finally, I wish to express my great appreciation to Mr. Yuang-Chyi Liang who was responsible for the construction of system circuits and many detailed tests.

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語言教室微電腦考試系統之設計

黃國恩

摘要

本文係針對目前國內現有之語言教學設備所設計之一套以AIM65為基礎之考試系統，供教學者對學生之聽力能進行即時之測驗而瞭解學生之進度。文中第一段係分析本校現有之國際牌LS電路，找出主機與副機間之獨立通訊電路。其次設計調變信號用之發射機與電腦問之介面。第二面則設計軟體解調用程式，交談式使用者軟體介面以及數學運算單元。本系統共用3.5K記憶完成其監督工作。
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